NAME OF THE FACULTY : Manju

DISCIPLINE : ECE

SEMESTER : 3rd

SUBJECT : DIGITAL ELECTRONICS

LESSON PLAN DURATION : Approx.15 weeks (from 30 July 2026 to 23 Nov.2026)

WORK LOAD (LECTURE/PRACTICAL) PER WEEK (IN HOURS):- Lecture-**03**, Practical-**04** Per Group

WEEK	THEORY		PRACTICAL		
	Lecture / Hrs	**TOPIC(Including Assignment/Test)**	**Practical / Hrs**		**Experiment**
1st	1	Introduction about Subject	GP-1		Introduction about Practical as per syllabus
	2	**UNIT-I: Number System and Codes** **Introduction to** analog and digital signal.	GP-2		Introduction about Practical as per syllabus
	3	Binary, octal and hexadecimal number system			
2nd	4	Conversion from decimal and hexadecimal to binary and vice-versa.	GP-1		verification and interpretation of truth tables FOR AND, OR, NOT NAND, NOR, EXOR and EXNOR gates
	5	Binary addition and subtraction Including binary points. 1's and 2's complement method of addition/ subtraction	GP-2		verification and interpretation of truth tables FOR AND, OR, NOT NAND, NOR, EXOR and EXNOR gates
	6	Concept of code, weighted and non-weighted codes, Examples of 8421, BCD, excess-3 and Gray code			
3rd	7	Concept of parity, single and double parity and error detection	GP-1		Realisation of logic functions with the help of NAND or NOR gates
	8	**Unit-II: Logic Gates and logic simplification:** Concept of negative and positive logic, Definition, symbols and truth tables of NOT, AND, OR Gates	GP-2		Realisation of logic functions with the help of NAND or NOR gates
	9	Definition, symbols and truth tables of NAND, NOR, EXOR Gates			
4th	10	NAND and NOR as universal gates.	GP-1		To design a half adder using XOR and NAND gates and verification of its operation
	11	Introduction to TTL and CMOS logic families	GP-2		To design a half adder using XOR and NAND gates and verification of its operation
	12	Postulates of Boolean algebra, De Morgan's Theorems, Implementation of Boolean			

5th	13	Karnaugh map (up to 4 variables)	GP-1		To design a full adder circuit using XOR and NAND gates and verify its operation
	14	Simple application in developing combinational logic circuits **Assignment-1**	GP-2		Construction of a full adder circuit using XOR and NAND gates and verify its operation
	15	**Sessional Test-1**			
6th	16	**Unit-III : Combinational Circuits:** Half adder and Full adder circuit, design and implementation	GP-1		To design circuit for 7-segment display
	17	4 bit adder circuit	GP-2		To design circuit for 7-segment display
	18	Four bit decoder circuits for 7 segment display and decoder/driver ICs			
7th	19	Basic functions and block diagram of MUX and DEMUX with different ICs	GP-1		Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops
	20	Basic functions and block diagram of Encoder	GP-2		Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops
	21	**UNIT-IV: Sequential Circuits** Concept and types of latch with their working and applications			
8th	22	Operation using waveforms and truth tables of RS, T, D,.	GP-1		Verification of truth table for encoder and decoder.
	23	Master/Slave JK flip flops	GP-2		Verification of truth table for encoder and decoder.
	24	Difference between a latch and a flip flop.			
9th	25	Introduction to Asynchronous counters and Synchronous counters, Binary counters,	GP-1		Verification of truth table for Multiplexer and De-Multiplexer
	26	Divide by N ripple counters	GP-2		Verification of truth table for Multiplexer and De-Multiplexer
	27	Divide by N ripple counters			
10th	28	Decade counter	GP-1		To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation
	29	Ring counter **Assignment-2**	GP-2		To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation
	30	**Sessional Test-2**			

11th	31	Introduction and basic concepts including shift left and shift right.	GP-1		To design a 4 bit ring counter and verify its operation
	32	Serial in parallel out, serial in serial out			
	33	Parallel in serial out, parallel in parallel out.	GP-2		To design a 4 bit ring counter and verify its operation
12th	34	Universal shift register.	GP-1		Use of Asynchronous Counter ICs (7490 or 7493)
	35	**UNIT-5: Converters and Memories** Working principle of A/D and D/A converter			
	36	Brief idea about different techniques of A/D converter and study of Stair step A/D Converter.	GP-2		Use of Asynchronous Counter ICs (7490 or 7493)
13th	37	Dual Slope A/D converter, Successive Approximation A/D Converter	GP-1		To design and verification of A/D converter
	38	Working p Detail study of : Binary Weighted D/A converter.			
	39	R/2R ladder D/A converter. Applications of A/D and D/A converter	GP-2		To design and verification of A/D converter
14th	40	**Semiconductor Memories:** Memory organization, classification of Semiconductor memories	GP-1		To design and verification of A/D converter
	41	(RAM, ROM, PROM, EPROM, EEPROM			
	42	static and dynamic RAM	GP-2		To design and verification of A/D converter
15th	43	Introduction to 74181 ALU IC **Assignment- 3**	GP-1		To design and verification of 74181 ALU
	44	**Sessional Test- 3**			
	45	Revision	GP-2		To design and verification of 74181 ALU